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First Named Inventor	John Robertson Tower et al.
Art Unit	2811
Examiner Name	Samuel A. Gebremariam
Attorney Docket No.	SAR 14108

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/Declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below): PTO-2038

Remarks:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln. No:	09/942,835
Appellant:	John Robertson Tower et al.
Filed:	August 30, 2001
Title:	CCD IMAGER CONSTRUCTED WITH CMOS FABRICATION TECHNIQUES AND BACK ILLUMINATED IMAGER WITH IMPROVED LIGHT CAPTURE
TC/A.U.:	2811
Examiner:	Samuel A. Gebremariam
Confirmation No.:	9999
Notice of Appeal Filed:	July 12, 2005
Docket No.:	SAR-14108

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
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Alexandria, VA 22313-1450

S I R :

In response to the Official Action dated June 2, 2005, Appellant is submitting this Appeal Brief for the above-identified application.

I. REAL PARTY IN INTEREST

The Real Party in Interest in this matter is Sarnoff Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative, or Assignee which may be related to, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 3, 7-11, 13-18, 20, 21, 31 and 32 are pending in this application. Claims 1, 3, 7-11, 13-18, 20, 21, 31 and 32 stand rejected. Claims 1, 3, 7-11, 13-18, 20, 21, 31

and 32 are appealed. Of those claims currently under appeal, claims 1, 7, 11, 16, 17, 18 and 20 are independent.

IV. STATUS OF AMENDMENTS

The present application is under final rejection. Appellant elected not to submit a Response After Final under 37 C.F.R. §1.116. Instead, Appellant filed a Notice of Appeal on July 12, 2005. The present application has been subject to a restriction requirement and rejected six times. Prior to the final rejection, Appellant filed a Response to the Restriction Requirement, an Amendment, an Amendment after Final, A Request for Continued Examination, an Amendment, an Amendment after Final, another Request for Continued Examination, an Amendment and a Notice of Appeal. In addition, Appellant's Attorney conducted a telephone interview with the Examiner and his supervisor on August 24, 2005. All of the Amendments were entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1, 3, 7-11, 13-18, 20, 21, 31 and 32 are appealed. The claimed invention is directed to a charge coupled device (CCD) that is made using standard complementary metal oxide semiconductor (CMOS) process techniques. This allows the formation of CCD circuitry, for example imaging and transfer devices, on the same integrated circuit as CMOS circuitry, for example an analog-to-digital converter. Due to design constraints on CCD devices it has been difficult or impossible to form CCD devices in a manner compatible with a CMOS process. The subject invention solves this problem.

In accordance with 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in each of the seven independent claims (1, 7, 11, 16, 17, 18 and 20) under appeal is set for the below. Citations to the application's support for claimed subject matter

are made by reference to numbered paragraph (¶) of Appellant's specification (*AS*) as originally filed (e.g., *AS* ¶ 6) as well as corresponding figures (Figs.). To improve the readability of the text, the quoted claim language is shown in **bold** type without quotation marks. The subject invention is described in terms of several embodiments, for the sake of brevity, each claim is described in terms of one embodiment. This description is not limiting as the claim covers other embodiments than the one described.

Claim 1

Independent claim 1 recites **a charge coupled device that is made according to a standard CMOS process** (*AS* ¶ 37) **on a substrate of a first conductivity type,** (110" Fig. 4D, *AS* ¶ 64 in Figure 4D, the substrate is shown as being a lightly-doped N-type substrate (N-)) **the charge coupled device comprising: a dielectric layer** (101 Fig. 4A) **overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer** (*AS* ¶¶ 40, 63), **at least two gate electrodes** (104, 104' Fig. 4D), **overlying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells in the substrate of the first conductivity type in response to bias potential applied to the gate electrodes** (*AS* ¶¶ 54, 63, *AS* ¶ 54 describes the operation of the device with respect to Fig. 4A "[d]uring the integration period, the potential on the transfer electrode 104' is kept at a value to hold the accumulated photoelectrons in the channel beneath the photogate 104." *AS* ¶ 63 states that the device shown in Fig. 4D operates in the same way as the device shown in Fig. 4A), **the at least two gate electrodes being separated by an inter-electrode gap** (210 Fig. 4D) **in the substrate of the first conductivity type** (*AS* ¶¶ 47, 48, these paragraphs describe methods for stabilizing the inter-electrode gap. *AS* ¶ 48 describes the purpose of this stabilization as being to "compensate for the potential charge barrier which may arise in the electrode gap

region." One skilled in the art would recognize that this charge barrier develops beneath the surface of the substrate and thus, that the inter-electrode gap, as the term is used in the specification, extends into the substrate); **apparatus for stabilizing the inter-electrode gap, selected from a group consisting of a semiconductor region of the first conductivity type** (494, Fig. 4D) **formed in the inter-electrode gap but having a different dopant concentration than the substrate** (*AS* ¶ 64 this paragraph defines item 494 (see specification amendment dated March 10, 2005) as being "a self-aligned N-- implant." As would be understood by the ordinarily skilled person, the designation "N--" indicates a very lightly doped N-type region. Thus the implant has a different dopant concentration than the N- substrate 110" in which it is implanted); **and means** (15 Fig. 1, and IG', Φ'_{TR}, Fig. 4C, *AS* ¶ 66) **for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes** (*AS* ¶ 47 describes this method for stabilizing the gap. the timing circuitry 15 is described as generating the clock signals for the device. Fig. 6 and *AS* ¶ 66 describe the operation of the device in Fig. 4A in terms of the timing diagram of Fig. 6. In Fig. 6. signals IG and Φ_{TR} are described as pulse signals. Thus, the ordinarily skilled person would understand that these signals are generated by the timing circuitry 15).

Claim 7

Independent claim 7 recites **a charge coupled device made according to a standard CMOS process** (*AS* ¶ 37) **on a substrate of a first conductivity type,** (110" Fig. 4D, *AS* ¶ 64, in Figure 4D, the substrate is shown as being a lightly-doped N-type substrate (N-)) **the charge coupled device comprising a dielectric layer** (101 Fig. 4A) **over the substrate** (*AS* ¶¶ 40, 63), **at least two gate electrodes** (104, 104' Fig. 4D)

overlying the dielectric layer, the at least two gate electrodes defining at least two charge wells in the substrate in response to bias potential applied to the gate electrodes, (*AS* ¶¶ 54, 63, *AS* ¶ 54 describes the operation of the device with respect to Fig. 4A "[d]uring the integration period, the potential on the transfer electrode 104' is kept at a value to hold the accumulated photoelectrons in the channel beneath the photogate 104." *AS* ¶ 63 states that the device shown in Fig. 4D operates in the same way as the device shown in Fig. 4A), **the at least two gate electrodes being separated by an inter-electrode gap** (210 Fig. 4D), **and; means for stabilizing the inter-electrode gap including means,** (15, Fig. 1, and IG', Φ'_{TR}, Fig. 4C, *AS* ¶ 66) , **for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes** (*AS* ¶ 47) **to stabilize the inter-electrode gap by preventing charge barriers from interfering with charge transfer between adjacent gate electrodes (***AS* ¶¶ 47, 48. *AS* ¶ 47 describes this method for stabilizing the gap. the timing circuitry 15 is described as generating the clock signals for the device. Fig. 6 and *AS* ¶ 66 describe the operation of the device in Fig. 4A in terms of the timing diagram of Fig. 6. In Fig. 6. signals IG and Φ_{TR} are described as pulse signals. Thus, the ordinarily skilled person would understand that these signals are generated by the timing circuitry 15).

Claim 11

Independent claim 11 recites **an optical sensor circuit for receiving photocarriers from a source and being formed on a single monolithic substrate** (110 Fig. 4A *AS* ¶¶ 38, 53. *AS* ¶ 38 describes the semiconductor substrate and *AS* ¶ 53 describes the optical sensor circuit) **comprising: a charge coupled device (CCD) array,**

the array being formed of a plurality of single polysilicon CMOS pixels (*AS* ¶¶ 40 and 53 describe the pixels as being constructed from a single polysilicon process) **each pixel including, a semiconductor layer of a first conductivity type** (100 Fig. 4A, *AS* ¶ 39. This is an N-well formed in the P-type epitaxial substrate) formed on the substrate) **a first dielectric layer** (101 Fig. 4A) **overlying the semiconductor layer, the first dielectric layer being a CMOS gate dielectric layer** (*AS* ¶¶ 40, 63); **at least two gate electrodes** (104, 104' Fig. 4A) **overlaying the first dielectric layer and configured to define at least two charge wells, respectively, in the semiconductor layer in response to a bias potential applied to the at least two gate electrodes** (*AS* ¶ 54, describes the operation of the device with respect to Fig. 4A "[d]uring the integration period, the potential on the transfer electrode 104' is kept at a value to hold the accumulated photoelectrons in the channel beneath the photogate 104.") **wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap** (210 Fig. 4A) **in the semiconductor layer**, (*AS* ¶¶ 47, 48, these paragraphs describe methods for stabilizing the inter-electrode gap. *AS* ¶ 48 describes the purpose of this stabilization as being to "compensate for the potential charge barrier which may arise in the electrode gap region." One skilled in the art would recognize that this charge barrier develops beneath the surface of the substrate and thus, that the inter-electrode gap, as the term is used in the specification, extends into the substrate) **a combination of one of the at least two charge wells and its overlapping gate electrode** (104 Fig. 4A) **forming a photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlying gate** (104' Fig. 4A,) **forming a transfer gate** (*AS* ¶ 53 at line 4 defines these structures); **and apparatus for stabilizing the inter-electrode gap selected from a group consisting of: a semiconductor region of the first conductivity type** (414, Fig. 4A, *AS* ¶ 53)

formed in the inter-electrode gap but having a different dopant concentration than the semiconductor layer (*AS* ¶¶ 53, 54, *AS* ¶ 53 defines item 414 as being "an optional N-- implant." As would be understood by the ordinarily skilled person, the designation "N--" indicates a very lightly doped N-type region Thus the implant has a different dopant concentration than the N well 100 (AS ¶ 54) in which it is implanted); **and means** (15, Fig. 1, and IG, Φ'_{TR}, Fig. 4A) **for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes** (*AS* ¶ 47 describes this method for stabilizing the gap. the timing circuitry 15 is described as generating the clock signals for the device. Fig. 6 and *AS* ¶ 66 describe the operation of the device in Fig. 4A in terms of the timing diagram of Fig. 6. In Fig. 6. signals IG and Φ_{TR} are described as pulse signals. Thus, the ordinarily skilled person would understand that these signals are generated by the timing circuitry 15).

Claim 16

Independent claim 16 recites **an imager system comprising: a single monolithic integrated circuit** (10, Fig. 1, *AS* ¶ 30) **including: a charge coupled device (CCD) imager array** (12, Fig. 1); **and a complementary metal oxide semiconductor (CMOS) analog to digital converter** (18, Fig. 1) **coupled to receive image signals from the CCD imager array** (*AS* ¶ 30 recites that the "system-on-a-chip (SOC) 10 is formed as a single semiconductor integrated circuit using a single standard CMOS process. The exemplary SOC 10 includes a CCD imager array 12, timing circuitry 15, optional row select circuitry 14, optional column select circuitry 13 and optional column reading circuitry 16, an analog-to-digital converter (ADC) 18 and digital gain circuitry 20").

Claim 17

Independent claim 17 recites **an imager system comprising: a single monolithic integrated circuit** (10, Fig. 1 *AS* ¶ 30) **including: a charge coupled device (CCD) imager array** (12, Fig. 1); **a complementary metal oxide semiconductor (CMOS) analog to digital converter** (18, Fig. 1) **coupled to receive image signals from the CCD imager array** (*AS* ¶ 30 recites that the "system-on-a-chip (SOC) 10 is formed as a single semiconductor integrated circuit using a single standard CMOS process. The exemplary SOC 10 includes a CCD imager array 12, timing circuitry 15, optional row select circuitry 14, optional column select circuitry 13 and optional column reading circuitry 16, an analog-to-digital converter (ADC) 18 and digital gain circuitry 20"); **and optics** (50 Fig. 1A) **configured to focus radiation on the CCD imager array** (AS ¶ 35 describes "an optics section that focuses radiation onto the imager array 12 of the SOC 10)..

Claim 18

Independent claim 18 recites **a charge coupled device made according to a standard single polysilicon CMOS process** (AS ¶ 40) **the charge coupled device comprising: a substrate of a first conductivity type** (110 Fig. 4A *AS* ¶ 38 describes the semiconductor substrate) **a well region of a second conductivity type opposite to the first conductivity type**, (100 Fig. 4A, AS ¶ 38 describe "a silicon wafer substrate having a first N or P (negative or positive) conductivity type. Charge wells having a second, opposite P or N conductivity type are formed in the substrate"); **an oxide layer, being a CMOS oxide layer** (101 Fig. 4A, *AS* ¶ 40 "[t]he transmission channel 100 is formed as a CMOS N-well, the oxide layer is a CMOS gate oxide and the electrodes are first or only polysilicon layer of the CMOS process); **first and second polysilicon gate electrodes** (104, 104' Fig. 4A, *AS* ¶ 40) **formed on the oxide layer over the well region, the first and second**

gate electrodes being separated by an inter-electrode gap (210 Fig. 4A) **in the well region** (*AS* ¶¶ 47, 48, these paragraphs describe methods for stabilizing the inter-electrode gap. *AS* ¶ 48 describes the purpose of this stabilization as being to "compensate for the potential charge barrier which may arise in the electrode gap region." One skilled in the art would recognize that this charge barrier develops beneath the surface of the N-well and thus, that the inter-electrode gap, as the term is used in the specification, extends into the N-well), **wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register** (*AS* ¶ 54); **and apparatus for stabilizing the inter-electrode gap selected from a group consisting of: a semiconductor region of the first conductivity type, formed in the inter-electrode gap but having a different dopant concentration than the semiconductor layer** (*AS* ¶¶ 53, 54, *AS* ¶ 53 defines item 414 as being "an optional N-- implant." As would be understood by the ordinarily skilled person, the designation "N--" indicates a very lightly doped N-type region Thus the implant has a different dopant concentration than the N well 100 (AS ¶ 54) in which it is implanted); **and means** (15, Fig. 1, and IG, Φ'_{TR}, Fig. 4A) **for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes** (*AS* ¶ 47 describes this method for stabilizing the gap. the timing circuitry 15 is described as generating the clock signals for the device. Fig. 6 and *AS* ¶ 66 describe the operation of the device in Fig. 4A in terms of the timing diagram of Fig. 6. In Fig. 6. signals IG and Φ_{TR} are described as pulse signals. Thus, the ordinarily skilled person would understand that these signals are generated by the timing circuitry 15).

Claim 20

Independent claim 20 recites **a back illuminated imager** (*AS* ¶¶ 60, 61), **comprising a substrate of a first conductivity type** (110" Fig. 4D, described in *AS* 64 as an N- substrate) **having a front side and a back side; a photodetector** (104, Fig. 4D, *AS* ¶ 58 describes the photogate with reference to Fig. 4A, *AS* 63 states that the pixel cell in Fig. 4D operates in the same way as the cell shown in Fig. 4A) **formed on the front side of the substrate** (thus the top of the device shown in Fig. 4D is the front side and the bottom is the back side)**; a well region of a second conductivity type** (493 Fig. 4D, *AS* ¶ 63 recites P wells 492 and 493) **opposite to the first conductivity type formed on the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction** (*AS* ¶ 63 recites that the PN junction is formed between the N- substrate and the P wells)**; and at least one diffusion region** (495, 497, 497 Fig. 4D, *AS* ¶ 64 defines these as N+ diffusion regions formed in the P wells 492 and 493) **in the well region of the second conductivity type forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction** (*AS* ¶¶ 60, 61, 63 describe this feature of the invention).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 18 is objected to due to informalities, claims 1, 11 and 18 are rejected under 35 U.S.C. § 112, second paragraph, claims 1 and 32 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent no. 4,952,523 to Fujii et al. (Fujii), claims 20 and 21 are rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent no. 6,489,992 to Savoye (Savoye), claims 3, 7, 8-11, 13-15, 18 and 31 are rejected under 35 U.S.C. § 103(a) as

being obvious in view of Fujii and U.S. patent no. 5,210,433 to Ohsawa et al. (Ohsawa) and claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. patent no. 6,088,057 to Hieda (Hieda) in view of Fujii..

VII. ARGUMENT

A. ARGUMENT SUMMARY

1. Appellant's claim 18 is not subject to objection or rejection under 35 U.S.C. § 112, second paragraph, because the term "single polysilicon" is a term that would be understood by one of ordinary skill in the semiconductor processing art.

2. Claims 1, 11 and 18 are not subject to rejection under 35 U.S.C. § 112, second paragraph because, Appellants have, by consistent use, defined the term "inter-electrode gap" to be a gap between the two gate electrodes that extends into the substrate or semiconductor well.

3. Claims 1 and 32 are not subject to rejection under 35 U.S.C. § 102(b) as being anticipated by Fujii because Fujii does not disclose or suggest that the implant is of the same conductivity type as the substrate.

4. Claims 20 and 21 are not subject to rejection under 35 U.S.C. § 102(e) in view of Savoye because Savoye does not disclose or suggest a well region that both includes a component of the back illuminated imager and that forms a p-n junction with the substrate which shields the component from photocarriers.

5. Claims 3, 7, 8-11, 13-15, 18 and 31 are not subject to rejection under 35 U.S.C. § 103(a) in view of Fujii and Ohsawa because neither Fujii, Ohsawa nor their combination disclose or suggest the specific gap stabilization structures claimed in independent claims 3,

11 and 18 either literally or inherently. Furthermore, the combination of Fujii and Ohsawa is improper. The remaining claims depend from the independent claims and are not subject to rejection for at least the same reasons.

6. Claims 16 and 17 are not subject to rejection under 35 U.S.C. § 103(a) in view of Hieda and Fujii because neither of these references nor their combination discloses or suggests a CCD imager and a CMOS analog-to-digital converter formed on a single monolithic integrated circuit.

B. ISSUES

Claim 18 stands objected to as including an informality. Claims 1, 11 and 18 stand rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 1 and 32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fujii. Claims 20 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Savoye. Claims 3, 7, 8-11, 13-15, 18 and 31 stand rejected under 35 U.S.C. § 103(a) as being obvious in view of Fujii and Ohsawa. Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being obvious in view of Hieda and Fujii. These are the only rejections; there are no other rejections and no other applied references. Thus, these objections and rejections define the issues on appeal.

C. LEGAL STANDARD

The legal standard for the objection to claim 18 appears to be MPEP §702.01 Obviously Informal Cases. This does not directly apply, however, as it is limited to situations in which it is "impractical to give a complete action on the merits because of an informal or insufficient disclosure...." Indeed, in this section, it is asserted that for claims,

"The claims should be rejected as failing to define the invention in the manner required by 35 U.S.C. 112 if they are informal." Accordingly, Appellants assert that the Examiner erred in asserting that claim 18 includes informalities and that the "objection" should have been a rejection under 35 U.S.C. § 112, second paragraph.

> 35 U.S.C. § 112 Specification
>
> ...
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
>
> 35 U.S.C. 102 Conditions for Patentability; Novelty and Loss of Right to Patent.
>
> A person shall be entitled to a patent unless –
>
> ...
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States,... .
>
> ...
>
> (e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language
>
> 35 U.S.C. 103 Conditions for Patentability; Nonobvious Subject Matter.
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

D. APPELLANT'S CLAIM 18 IS NOT SUBJECT TO OBJECTION OR REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH BECAUSE THE TERM "SINGLE POLYSILICON" IS A TERM THAT WOULD BE UNDERSTOOD BY ONE OF ORDINARY

SKILL IN THE ART.

Claim 18 does not include any informalities and it particularly points out and distinctly claims the invention as the term "single polysilicon CMOS process" is understood in the art to be a process for manufacturing CMOS devices that employs one polysilicon growth step. This is a well-known term in the art. In support of this assertion, Appellants cite U.S. patent no. 6,104,277 which, at column 1, line 19 refers to a "conventional single-polysilicon CMOS process." In addition, Appellants note that a search of the Patent Office Database of Issued Patents made on August 25, 2005 lists 38 patents that include the term "single polysilicon" in their titles Thus, Appellants assert that the term "single polysilicon" is not a typographical error but, instead is a term of art that would be understood by one of ordinary skill in the art. Accordingly, claim 18 is not subject to objection or to rejection under 35 U.S.C. § 112, second paragraph.

E. CLAIMS 1, 11 AND 18 ARE NOT SUBJECT TO REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH BECAUSE, APPELLANTS HAVE, BY CONSISTENT USE, DEFINED THE TERM "INTER-ELECTRODE GAP" TO BE A GAP BETWEEN THE TWO GATE ELECTRODES THAT EXTENDS INTO THE SUBSTRATE OR SEMICONDUCTOR WELL.

It is settled law that "a patentee is free to be his own lexicographer."[1] Furthermore, it is settled law that a term may be defined by consistent usage of the claim term in the specification, "Thus, when a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term

[1]*Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980, 34 USPQ2d 1321, 1329-30 (Fed. Cir. 1995).

'by implication.'"[2] In the Office Action, it was asserted that the phrase "inter-electrode gap in the substrate" in claims 1, 11 and 18 is indefinite because "[t]he inter-electrode gap is a gap (empty space). It is not clear how one forms a semiconductor region of first conductivity type in an empty space." This definition by the examiner assumes that the only definition of "gap" is "empty space." It is noted, however, that this definition is not found in the dictionary. Instead, "gap" is defined as "a break in a barrier" or "a separation in space" or "a break in continuity."[3] The subject application consistently uses the term "gap" to mean a discontinuity or a separation in space. There is no indication in the definition or in the subject application that this separation is "empty space."

Indeed, at *AS* ¶ 61, Appellants describe the barrier gaps 463 of Fig. 4C as follows:

> In the embodiment of the invention shown in Fig. 4C, the polysilicon gates 104 and 104' are configured to provide barrier gaps 463 between the P well 464 and the N-well barrier diffusion 462. The barrier gaps 463 separate the P-channel from the blooming drain formed by the N-well 462 and P+ diffusion 460.

This passage clearly describes the barrier gaps 463 as extending into the substrate. Similarly, the application includes many references to "stabilizing the inter-electrode gap." The reason for this stabilization is to "[compensate] for the potential charge barrier which may arise in the electrode gap region 210." (*AS* ¶ 48). One of ordinary skill in the are would understand that this charge barrier is not in "empty space" between the polysilicon gates 104 and 104' but within the substrate or semiconductor well beneath the separation between the gates 104 and 104'. A charge barrier requires an accumulation of electronic charge. Electronic charge can not accumulate in empty space. Thus, the inter-electrode gap necessarily extends into the substrate or semiconductor well. Other references that

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[2] *Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1270, 59 USPQ2d 1865, 1872 (Fed. Cir. 2001).
[3] *Webster's Ninth New Collegiate Dictionary*, Merriam-Webster, Inc. Springfield MA p.505 (1983)

show the use of the word "gap" as a discontinuity extending into the substrate or semiconductor well include *AS* ¶ 50, "Although the P+ diffusions 308 are shown as filling only part of the gap between the gate electrodes 104, it is contemplated that they may entirely fill the gap," and *AS* ¶ 53 "the inter-electrode gap may be stabilized by applying suitable biases to the gate electrodes 104 and 104' to cause fringing fields from the gate electrodes to extend into the gap." One of ordinary skill in the art would understand that the fringing fields generated by applying suitable biases to the gate electrodes would not extend only laterally in the "empty space" between the electrodes 104 and 104' but would necessarily extend down into the substrate or semiconductor well.

Thus, because the specification has consistently used the terms "gap" and "inter-electrode gap" to indicate a discontinuity within the substrate or semiconductor well, the term is used appropriately in claims and claims 1, 11 and 18 are not subject to rejection under 35 U.S.C. § 112, second paragraph.

F. APPELLANT'S INVENTION AS RECITED IN CLAIMS 1 AND 32 IS NOVEL OVER THE DISCLOSURE OF FUJII BECAUSE FUJII DOES NOT DISCLOSE OR SUGGEST THAT THE IMPLANT IS OF THE SAME CONDUCTIVITY TYPE AS THE SUBSTRATE.

It is asserted in the Final Office Action that Fujii teaches "the at least two gate electrodes (42, 44) overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells (the n and p regions of the substrate), the at least two gate electrodes being separated by an inter-electrode gap (the gap between 42 and 44) and apparatus for stabilizing the inter-electrode gap, is a semiconductor region (36) of the first conductive type but having a different dopant concentration than region (32), in the inter-electrode gap."

Appellants respectfully disagree with this assertion. Fujii clearly shows in FIGs. 8 and 9 that the second p-type silicon region 36 (i.e., which the Examiner corresponds to the semiconductor region of the first conductive type recited in claim 1) is of opposite type to the n-type material in which the charge wells are formed. The subject invention, as defined by claim 1, requires that the charge wells formed by the gate electrodes be formed *in the substrate of the first conductivity type* and that t*he stabilizing implant also be of the first conductivity type*. Fujii does not meet this limitation because, in Fujii, the charge wells are formed in the n-type layer 32 while the implants 36 are p-type implants. This claim limitation is illustrated in Fig. 4D of the subject application in which the charge wells are formed in the n-type region 110" and the stabilizing implant is an n-- implant 494. (*AS* ¶ 64 as amended in the amendment dated March 10, 2005).

In addition, Fujii fails to disclose that the dielectric layer overlying at least a portion of the substrate is a CMOS gate dielectric layer. Indeed, Fujii relates to a CCD process. As set forth in the subject application at *AS* ¶ 7, however, CCD and CMOS processes are incompatible. An advantage of the subject invention is that it allows CCD devices to be built using standard CMOS process techniques. As defined by claim 1, a CMOS gate dielectric layer is the dielectric layer of the charge-coupled device. Accordingly, the use of a CMOS gate electrode provides the subject invention with an advantage over Fujii. Because, as set forth in the subject specification, CMOS and CCD devices are incompatible, it would not have been obvious to the skilled person to make the dielectric layer in Fujii as a CMOS gate dielectric layer.

In response to this argument, the Examiner relies on the rejection under 35 U.S.C. § 112, second paragraph to assert that the claim is invalid. Thus, the rejection does not address the assertion that this limitation is not taught in the prior art. Accordingly,

Appellants contend that the Examiner concedes that this limitation is not taught in the prior art. It is further asserted in the Final Office Action that the statement in the claim that the dielectric layer is "a CMOS gate dielectric layer, made using a standard CMOS process is given no patentable weight because it is considered a product-by-process claim. It is the patentability of the claimed product and not of recited process steps, which must be established." Appellants respectfully disagree with this analysis. The claim term in question states: "a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer." This statement does not involve any process steps but defines the dielectric layer as being a CMOS gate dielectric layer. One of ordinary skill in the art would understand the characteristics and properties of a CMOS gate dielectric layer. See, for example, *AS* 69 "The metal layer may cover an area just beyond the gap or may cover a larger surface having a range to where the metal electrodes are separated by a distance corresponding to a minimum design feature of the CMOS process. In the embodiment of the invention shown in Fig. 7, the dielectric layer 312 is a gate-oxide layer and, so, is relatively thin."

As claim 1 requires the substrate to be formed of the first conductivity type, the charge wells to be formed in the substrate, the implant layer to be also of the first conductivity type and to be formed in the inter-electrode gap, and the dielectric layer to be a CMOS gate dielectric layer, claim 1 recites structure that is not found in Fujii. Accordingly, claim 1 is not subject to rejection as being anticipated by Fujii.

Dependent claim 32 includes all of the features of claim 1 from which it depends. Thus, claim 32 is not subject to rejection under 35 U.S.C. § 102(b) as being anticipated by Fujii for at least the same reasons as claim 1.

G. APPELLANT'S INVENTION AS RECITED IN CLAIMS 20 AND 21 IS NOT ANTICIPATED BY SAVOYE BECAUSE SAVOYE DOES NOT DISCLOSE OR SUGGEST A WELL REGION THAT BOTH INCLUDES A COMPONENT OF THE BACK ILLUMINATED IMAGER AND THAT FORMS A P-N JUNCTION WITH THE SUBSTRATE WHICH SHIELDS THE COMPONENT FROM PHOTOCARRIERS.

In the Office Action, it is asserted that Savoye teaches "a well region (420) of a second conductivity type, opposite to the first conductivity type (n region), formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction (refer to fig. 4B); and at least one diffusion region (400) in the well region of the second conductivity type forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from the photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction (refer to col. 16, lines 6-17)."

Contrary to the assertion by the examiner, Savoye teaches that the component of the back illuminated imager (i.e. the blooming drain 400) is formed in a buried channel 70, not in the heavily-doped p-type region 420. It is this heavily-doped P-type region, however, that shields the blooming drain from the photoelectrons. Thus, Savoye requires an extra step that is not used in the subject invention. Referring to Fig. 4D, the subject invention forms a p-well 493 in the n- substrate 110" and it is the junction between the p-well and the n- substrate that shields the n-type diffusion regions 495, 496 and 497, formed in the P-well, from the photocarriers. Savoye, on the other hand, forms the heavily-doped P-type regions 420, forms the buried channel 70 over these regions, and then forms the blooming drain 400 in the channel 70. Savoye needs an additional implant 420 to block the photocarriers from the blooming drain. This additional implant is not the same as the well

region of the subject invention because the subject invention requires that the component be formed in the well region. In Savoye, the component of the back illuminated imager is not formed in the region 420 but in the buried channel 70.

Furthermore, Savoye teaches that the p-n junction between the buried channel 70 and the substrate is insufficient to shield the blooming drain from the photoelectrons. (See col. 16, lines 14-17). Thus, Savoye teaches away from the invention defined by claim 20. Because the subject invention achieves the same effect without requiring the additional heavily-doped p-type region 420 required by Savoye, the subject invention represents an advantage over Savoye. Moreover, because Savoye teaches that the junction between the buried channel 70 and the substrate is not sufficient to shield the blooming drain 400, the skilled person would not be motivated to modify Savoye to meet the limitations of claim 20.

Because Savoye does not disclose or suggest a well region that both includes a diffusion forming a component of the back illuminated imager and that the well region forms a p-n junction with the substrate that shields the component from photocarriers, as required by claim 20, claim 20 is not subject to rejection under 35 U.S.C. § 102(e) in view of Savoye. Claim 21 depends from claim 20 and is not subject to rejection under 35 U.S.C. § 102(e) in view of Savoye for at least the same reasons as claim 20.

This argument was presented in the amendment dated March 10, 2005. In response to this argument, the Examiner, in the Final Office Action merely repeated the rejection. Accordingly, Appellant's arguments have not been addressed.

H. APPELLANT'S INVENTION AS RECITED IN CLAIMS 3, 7, 8-11, 13-15, 18 AND 31 IS NOT OBVIOUS IN VIEW OF FUJII AND OHSAWA BECAUSE NEITHER FUJII, OHSAWA NOR THEIR COMBINATION DISCLOSE OR SUGGEST THE SPECIFIC GAP STABILIZATION STRUCTURES CLAIMED IN INDEPENDENT CLAIMS 3, 11 AND 18 EITHER LITERALLY OR INHERENTLY. FURTHERMORE, THE COMBINATION OF FUJII AND OHSAWA IS IMPROPER.

The Fujii patent is described above and, for the sake of brevity, that description is not repeated here. Ohsawa et al. was cited as showing the further gate electrode overlying the further dielectric layer as required by claim 3, which depends from claim 1. The combination of Fujii and Ohsawa et al was cited as inherently disclosing the "means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes," as required by claims 1, 7, 11 and 18. Appellants respectfully disagree that the combination of Fujii and Ohsawa et al. inherently disclose this feature of claims 1, 7, 11 and 18. In particular, Appellants note that Ohsawa et al. disclose the further gate electrode overlying the further dielectric layer to control the inter-electrode gap. By disclosing this feature, Ohsawa et al. admit that their gate electrodes and driving circuitry do not form the fringing fields because, if it did, then the further gate electrode overlying the further dielectric layer would not be needed. Fujii discloses virtual gate regions 34 and 36, shown in Fig. 9, which have the effect of eliminating the need for stabilizing any inter-electrode gap, as described in Fig,. 3B and *AS* ¶¶ 50 and 51. As described at *AS* ¶ 50, virtual gate charge transfer devices are well-known in the art.

Because both Fujii and Ohsawa et al. disclose either structures that do not need to have inter-electrode gaps stabilized or other structures than the claimed structure for stabilizing the inter-electrode gap, the combination of these references can not "inherently" disclose the structures required by claims 1, 11 and 18.

The requirements for an item to be inherent in a disclosure are well settled. The CCPA had stated that "inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."[4] Furthermore, the inherent item must be immediately recognizable as such to the ordinarily skilled person, "To serve as an anticipation, when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill in the art."[5] That is, the missing element or function must *necessarily* result from the prior art reference(s). In this instance, because these references either 1) do not need to stabilize the inter-electrode gap or 2) disclose other methods than the claimed method to stabilize the gap, the skilled person would not recognize that the "means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes," as being inherently present in either reference or their combination.

Furthermore, Appellants continue to assert that the combination of Fujii and Ohsawa et al. is improper. "[T]he mere fact that a worker in the art could rearrange the part of the

[4] *In re Oelrich*, 666 F.2d. 578, 581, 212 USPQ 323, 326 (CCPA 1981)

reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary change in the reference device."[6]

A prima facie obviousness rejection requires that the modification of one reference be based on motivation evidenced in the record. Because the cited references either do not need to stabilize the inter-electrode gap or use other methods for stabilizing the gap, the cited art does not provide any suggestion or motivation to modify Fujii to control its gap potential by causing a fringing field to extend across the inter-electrode gap to stabilize the inter-electrode gap. Thus, the combination of Fujii and Ohsawa based on the rationale given by the Examiner is improper.

Accordingly, claims 1, 7, 11 and 18 are not subject to rejection as being unpatentable over Fujii in view of Ohsawa et al. Claims 3 and 8-10 depend from claim 1 and claims 13-15 and 31 depend from claim 11. Accordingly, these claims are not subject to rejection as being unpatentable over Fujii in view of Ohsawa et al. for at least the same reasons as their base claims.

These arguments were also made in the Amendment dated March 10, 2005. In the Final Office Action, the arguments on the merits were not addressed. Instead, the Examiner only addressed the propriety of combining the references.

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[5] *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 20 USPQ 2d 1746, 1749 (Fed. Cir. 1991).
[6] *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984)

I. CLAIMS 16 AND 17 ARE NOT SUBJECT TO REJECTION UNDER 35 U.S.C. § 103(A) IN VIEW OF HIEDA AND FUJII BECAUSE NEITHER OF THESE REFERENCES NOR THEIR COMBINATION DISCLOSES OR SUGGESTS A CCD IMAGER AND A CMOS ANALOG-TO-DIGITAL CONVERTER FORMED ON A SINGLE MONOLITHIC INTEGRATED CIRCUIT.

In response to this rejection, Appellants assert that neither Hieda, Fujii nor their combination disclose or suggest,

> a single monolithic integrated circuit including:
>
> a charge coupled device (CCD) imager array; and
>
> a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array

as required by claims 16 and 17. In the Final Office Action, it was asserted that Hieda discloses "a single monolithic integrated circuit including CCD imager (2) (fig.1) and a CMOS analog to digital converter (3)." Appellants respectfully disagree with this assertion. Hieda, at col. 3, lines 23-29 states:

> Referring to FIG. 1, this image pickup apparatus comprises an image pickup optical system 1 including an image pickup lens and a stop, a CCD 2 which is a color image sensor, and a digitization circuit 3 which converts a CCD output signal into a digital signal by using a sample-and-hold circuit, a gain variable amplifier, and an A/D converter. These components of the digitization circuit 3 are formed on a one-chip IC.

This statement by Hieda concerning the circuitry formed on the "one-chip IC" refers only to the components of the digitization circuit 3, not to the CCD 2. Thus, contrary to the statement in the Office Action, Hieda does not teach that a CCD imager and a CMOS analog-to-digital converter can be formed on a single monolithic integrated circuit. Furthermore, as set forth at *AS* ¶ 7 it is not feasible in the prior art to fabricate CCD devices using CMOS process techniques. Indeed, Hieda does not disclose forming the CCD devices and the CMOS devices on a single integrated circuit. Rather, it discloses forming them as separate

integrated circuits. Also, it is noted that the Fujii reference does not even mention CMOS, Complementary Metal Oxide Semiconductor or any similar circuitry. From the above, based on Hieda and Fujii, the skilled person would not understand that a CMOS analog-to-digital converter could be combined with a CCD imager on a single monolithic integrated circuit, as required by claims 16 and 17. Accordingly, claims 16 and 17 are not subject to rejection under 35 U.S.C. § 103(a) as being obvious in view of Hieda and Fujii.

This argument was made in the Amendment dated March 10, 2005. In response to this argument, the Examiner did not address the merits of the arguments but, instead responded as if Appellants had asserted that the combination of references was improper. Appellants did not make any such argument. Because Appellants' assertions that the basis of the Examiner's argument regarding the patentability of claims 16 and 17 are not opposed, Appellants assume that the Examiner agrees that these arguments are valid. Thus, claims 16 and 17 are in condition for allowance.

H. CONCLUSION

Appellant has addressed each of the nine grounds for objecting to or rejecting the claims of the above-identified application to show that these grounds are improper.

Accordingly, Appellants respectfully request the Board's reversal of these objections and rejection.

Respectfully submitted,

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Attachment: Pending Claims

Dated: September 12, 2005

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The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. 18-0350 of any fees associated with this communication.

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September 12, 2005

BETH JOHNSON

VIII. CLAIMS APPENDIX

1. A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells in the substrate of the first conductivity type, in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap in the substrate of the first conductivity type; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type, formed in the inter-electrode gap, but having a different dopant concentration than the substrate; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

2. (Canceled)

3. A charge coupled device according to claim 1, wherein the apparatus for stabilizing the inter-electrode gap further includes:

a further dielectric layer formed over the at least two gate electrodes; and

a further gate electrode formed overlying the further dielectric layer and selectively positioned over the inter-electrode gap.

4. - 6. (Canceled)

7. A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes defining at least two charge wells, in the substrate, in response to a bias potential applied to the at least two gate electrodes , the at least two gate electrodes being separated by an inter-electrode gap; and

means for stabilizing the inter-electrode gap including means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes to stabilize the inter-electrode gap by preventing charge barriers from interfering with charge transfer between adjacent gate electrodes.

8. A charge coupled device according to claim 1, wherein a first one of the charge well areas and its corresponding gate electrode form a photogate optical sensor and the charge coupled device further comprises:

a well region of a first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

9. A charge coupled device according to claim 8, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

10. A charge coupled device according to claim 9, wherein the plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

11. An optical sensor circuit for receiving photocarriers from a source and being formed on a single monolithic substrate comprising:

a charge coupled device (CCD) array, the array being formed of a plurality of single polysilicon CMOS pixels, each pixel including,

a semiconductor layer of a first conductivity type formed on the substrate;

a first dielectric layer overlaying the semiconductor layer, the first dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the first dielectric layer and configured to define at least two charge wells, respectively, in the semiconductor layer, in response to a bias potential applied to the at least two gate electrodes, wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap in the semiconductor layer, a combination of one of the at least two charge wells and its respective overlaying gate electrode forming a photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlaying gate electrode forming a transfer gate; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type, formed in the inter-electrode gap, but having a different dopant concentration than the semiconductor layer; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

12. (Canceled)

13. An optical sensor according to claim 11, further comprising:

a well region of the first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

14. An optical sensor according to claim 13, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

15. A charge coupled device according to claim 13, wherein the plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

16. An imager system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array.

17. A camera system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array; and

optics configured to focus radiation onto the CCD imager array.

18. A charge coupled device made according to a standard single polysilicon CMOS process, the charge coupled device comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type;

an oxide layer formed over at least the well region, the oxide layer being a CMOS gate oxide layer;

first and second polysilicon gate electrodes formed on the oxide layer over the well region, the first and second gate electrodes being separated by an inter-electrode gap in the well region, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region, but having a different dopant concentration than the well region; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

19. (Canceled)

20. A back illuminated imager comprising:

a substrate of a first conductivity type having a front side and a back side;

a photodetector formed in the front side of the substrate;

a well region of a second conductivity type, opposite to the first conductivity type, formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction; and

at least one diffusion region in the well region of the second conductivity type forming a component of the back illuminated imager;

whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction.

21. An electronic camera system comprising:

an imager formed according to one of claims 18 and 20; and

optics that are configured to focus radiation onto the imager.

22. - 30. (Canceled)

31. The charge coupled device of claim 11 , wherein the semiconductor layer is a transmission channel and the transmission channel is a CMOS N-well.

32. The charge coupled device of claim 1, wherein the at least two gate electrodes include at least two CMOS polysilicon gate electrodes.